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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,868	08/25/2003	Tatsuya Kawasaki	070639-0143	1667

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,868	KAWASAKI, TATSUYA	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/25/03, 02/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "115" has been used to designate both output of the test pattern generator and input into the selector in figure 11. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tatematsu (US 4,821,238) in view of Kawagoe et al. (US 2001/0056557 A1), Brown et al. (US 4,446,514) and Haraguchi (US 6,034,907).

As per claim 1, Tatematsu teaches a test circuit for a memory, which is incorporated into a semiconductor integrated circuit together with the memory and a test signal generating circuit for generating a test signal for said memory (fig. 6, col. 2, lines 46-48, col. 6, lines 25-37, Tatematsu).

However Tatematsu does not explicitly teach the specific use of a control circuit for conducting control of said test signal generating circuit and an initial data of the test signal and a control data for controlling said test signal generating circuit, which are input to said test signal generating circuit in said test setting mode.

Kawagoe et al. in an analogous art teach that control circuit 26 generates...external control signals (page 4, paragraph 80, Kawagoe et al.). Kawagoe et al. also teach that referring to FIG. 2...BIST control unit 2010 (page 4, paragraph 82, Kawagoe et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tatematsu's patent with the teachings of Kawagoe et al. by including an additional step of using a test signal generating circuit for generating a test signal for said memory, a control circuit for conducting control of said test signal generating circuit and an initial data of the test signal and a control data for controlling said test signal generating circuit, which are input to said test signal generating circuit in said test setting mode.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to control generation of test signal to test the memory.

Tatematsu also does not explicitly teach the specific use of using a first control signal input from outside and a control data to said control circuit are input serially from an identical terminal.

However Haraguchi in an analogous art teaches that the test signal...component circuits (col. 1, lines 49-53, Haraguchi).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tatematsu's patent with the teachings of Haraguchi by including an additional step of using a first control signal input from outside and a control data to said control circuit are input serially from an identical terminal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a first control signal input from outside and a control data to said control circuit are input serially from an identical terminal would provide the opportunity to apply control signals for memory testing using an external device.

Tatematsu also does not explicitly teach the specific use of switching a test setting mode and a test execution mode to each other.

However Brown et al. in an analogous art teach that the "1" from the register R14 is input into gate 669 together with a signal test initialization and the output of gate 669 is input into gate 684 together with the "0" that is input into Register 15 to define the ROM test. The output of gate 684 signifies the ROM test to be performed (fig. 35A, 35A', col. 34, lines 20-25, Brown et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tatematsu's patent with the teachings of Brown et al. by including an additional step of switching a test setting mode and a test execution mode to each other.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that switching a test setting mode and a test execution mode to each other would provide the opportunity to set up the initial test values in a test setting mode, then conduct the tests in a test execution mode.

5. Claims 2, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tatematsu (US 4,821,238), Kawagoe et al. (US 2001/0056557 A1), Brown et al. (US 4,446,514) and Haraguchi (US 6,034,907) as applied to claim 1 above, and further in view of Kishi et al. (US 5,987,635).

As per claim 2, Tatematsu, Kawagoe et al., Brown et al. and Haraguchi substantially teach the claimed invention described in claim 1 (as rejected above). Tatematsu also teaches a test circuit for a memory, wherein said test signal generating circuit comprising, an address signal generating circuit, a data signal generating circuit, and a read/write signal generating circuit (fig. 6, col. 6, lines 25-37, lines 59-63, Tatematsu).

However Tatematsu, Kawagoe et al., Brown et al. and Haraguchi do not explicitly teach the specific use of a chip select signal generating circuit.

Kishi et al. in an analogous art teach a chip select signal generator...memory circuit unit (col. 15, lines 13-17, Kishi et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tatematsu's patent with the teachings of Kishi et al. by including an additional step of using a chip select signal generating circuit.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a chip select signal generating circuit would provide the opportunity to select the memory chip required to be tested.

- As per claim 5, Tatematsu, Kawagoe et al., Brown et al., Haraguchi and Kishi et al. teach the additional limitations.

Kishi et al. teach the read/write signal generating circuit generates a read/write signal based on an output signal of said chip select signal generating circuit (col. 15, lines 13-17, Kishi et al.).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tatematsu (US 4,821,238), Kawagoe et al. (US 2001/0056557 A1), Brown et al. (US 4,446,514) and Haraguchi (US 6,034,907) as applied to claim 1 above, and further in view of Adams et al. (US 2003/0120974 A1).

As per claim 3, Tatematsu, Kawagoe et al., Brown et al. and Haraguchi substantially teach the claimed invention described in claim 1 (as rejected above). Tatematsu also teaches control of read/write circuit (fig. 6, col. 4, lines 21-23, col. 6, lines 59-63, Tatematsu). Haraguchi also teaches second, third and fourth control signals, respectively, which are input from outside (col. 1, lines 49-53, Haraguchi).

However Tatematsu, Kawagoe et al., Brown et al. and Haraguchi do not explicitly teach the specific use of increment and decrement of an address and presence of a data reverse.

Adams et al. in an analogous art teach Increment/Decrement Address (page 6, paragraph 84, Adams et al.). Adams et al. also teach reverse-checkerboard data pattern (page 8, paragraph 102, Adams et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tatematsu's patent with the teachings of Adams et al. by including an additional step of using increment and decrement of an address and presence of a data reverse.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using increment and decrement of an address and presence of a data reverse would provide the opportunity to use different combination of test vectors to test memory to find faults.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tatematsu (US 4,821,238), Kawagoe et al. (US 2001/0056557 A1), Brown et al. (US 4,446,514) and Haraguchi (US 6,034,907) as applied to claim 1 above, and further in view of Ono (JP 02216565 A).

As per claim 4, Tatematsu, Kawagoe et al., Brown et al. and Haraguchi substantially teach the claimed invention described in claim 1 (as rejected above).

However Tatematsu, Kawagoe et al., Brown et al. and Haraguchi do not explicitly teach the specific use of a selector for selecting an output data of a selected memory, and outputting it to outside as an output data.

Ono in an analogous art teaches that the selector applies the selected memory output data to a data comparator, and the data comparator compares the data with the test data set in a data register (abstract, Ono).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tatematsu's patent with the teachings of Ono by including an additional step of using a selector for selecting an output data of a selected memory, and outputting it to outside as an output data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a selector for selecting an output data of a selected memory, and outputting it to outside as an output data would provide the opportunity to determine test results in a selected memory circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
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